What is claimed is:

1. A MPEG video decoder comprising:

a picture decoding section for starting a decoding of a MPEG bit-streams for the predetermined number of pictures in response to a decoding start command, and outputting a decoding completion notification when the decoding of the bit-stream for said predetermined number of pictures is completed;

a decoding frame buffer for sequentially storing picture data decoded by said picture decoding section and outputting a bufferfull notification when a predetermined quantity of picture data is stored;

a decoding start command generating section for outputting said decoding start command when said decoding completion notification is outputted from said picture decoding section and said bufferfull notification is not outputted from said decoding frame buffer; and

a picture data output section for transmitting said picture data stored in said decoding frame buffer to a display unit.

2. The MPEG video decoder according to claim 1, wherein said picture data output section transmits said picture data to said display unit in synchronization with a vertical synchronous signal.

3. The MPEG video decoder according to claim 1, wherein said picture decoding section refers to the picture data stored in said decoding frame buffer,

thereby decoding other picture data.

4. The MPEG video decoder according to claim 1, wherein said MPEG bit-stream is inputted from either an ATM (Asynchronous Transfer Mode) transmission path or a storage medium to said picture decoding section via a bit-stream buffer.

5. The MPEG video decoder according to claim 1, wherein said picture data output section includes a display buffer for temporarily storing the picture data to be outputted to said display unit, and a display control section for transferring the picture data from said decoding frame buffer to said display buffer.

6. The MPEG video decoder according to claim 5, wherein said display control section suspends to transfer the picture data from said decoding frame buffer to said display buffer when a pause command is inputted thereto.

7. The MPEG video decoder according to claim 1, said MPEG video decoder further comprising:

an input terminal for receiving said MPEG bit-stream; and

a bit-stream buffer for temporarily storing said MPEG bit-stream inputted to said input terminal and outputting said MPEG bit-stream to said decoding frame buffer.

8. The MPEG video decoder according to claim 1, wherein said decoding start command generating section outputs said decoding start command in response to a

command from a outside apparatus, said decoding completion notification, and said bufferfull notification.

9. A MPEG video decoder comprising:

a picture decoding section for starting to decode a MPEG bit-stream in response to a decoding start command;

a decoding frame buffer for storing picture data decoded by said picture decoding section;

a display control section for analyzing parameters of the picture data for the predetermined number of pictures, said picture data being decoded by said picture decoding section, and controlling a transfer of said picture data from said decoding frame buffer to a display unit in accordance with an analysis result of said parameters; and

a decoding control section for outputting said decoding start command based on the parameters of said picture data.

10. The MPEG video decoder according to claim 9, wherein said display control section determines the number of display fields of each of said pictures based on said parameters for the predetermined number of pictures, and allowing said pictures to be displayed on said display unit for a predetermined period of time equivalent to said number of display fields.

11. The MPEG video decoder according to claim 10, wherein the parameters of said picture data include a peculiar play back flag.

12. The MPEG video decoder according to claim 11, wherein said peculiar play back flag is a repeat first field flag or a slow play back command flag.

13. The MPEG video decoder according to claim 10, wherein said display control section stores a table showing a relation between the parameters of said picture data and said number of display fields.

14. The MPEG video decoder according to claim 10, wherein said display control section includes four shift registers of a re-order register for storing a parameter of either an I picture or a P picture and a bank address thereof, a current register for storing a parameter of a picture and a bank address thereof, the picture being subsequently displayed, a field delay register for delaying the parameter and the bank address shifted from said current register by one field time, and a display register for storing a parameter of a picture and a bank address thereof, which is being displayed.

15. The MPEG video decoder according to claim 14, wherein said re-order register and said current register use said decoding start command as a shift pulse, and said field delay register and said display register use a vertical synchronous signal as a shift pulse.

16. The MPEG video decoder according to claim 14, said MPEG video decoder further comprising:

a status register for indicating states of said re-order register, said current register, said field delay

register and said display register.

17. The MPEG video decoder according to claim 16, wherein said decoding control section refers to a state of said status register, and issues said decoding start command when data is not existed in either said re-order register or said current register.

18. The MPEG video decoder according to claim 17, wherein said decoding control section refers to said status register at a timing in synchronization with a vertical synchronous signal.

19. The MPEG video decoder according to claim 16, wherein said display control section refers to a state of said status register, and determines said number of display fields from the parameter when the parameter and the bank address are stored in said display register.

20. The MPEG video decoder according to claim 19, wherein said display control section refers to said status register at a timing in synchronization with a vertical synchronous signal.

21. A MPEG video decoding method comprising the steps of:

decoding a MPEG bit-stream for the predetermined number of pictures, and storing the decoded bit-stream in a decoding frame buffer as picture data;

transferring the picture data for the predetermined number of pictures to a display unit, said picture data being stored in said decoding frame buffer;

suspending to decode the bit-stream when a predetermined quantity of picture data is stored in said decoding frame buffer; and

resuming to decode the bit-stream when a quantity of picture data is smaller than the predetermined quantity of picture data.

22. The MPEG video decoding method according to claim 21, wherein said picture data is transferred to said display unit at a timing in synchronization with a vertical synchronous signal.

23. A MPEG video decoding method comprising the steps of:

starting to decode a MPEG bit-stream in response to a decoding start command outputted from a decoding control section;

storing decoded picture data in a decoding frame buffer;

storing parameters of said decoded picture data in a display control section;

determining the number of display fields for each picture from said parameters by said display control section; and

displaying each of said pictures on a display unit for a period of time equivalent to the number of display fields.